APPENDIX 4

BEST AVAILABLE COPY

13.2

Variable Threshold-Voltage SOI CMOSFETs with Implanted Back-Gate Electrodes for Power-Managed Low-Power and High-Speed sub-1-V ULSIs

Tsuyoshi Kachi, Toru Kaga, Shoji Wakahara, and Digh Hisamoto

Central Research Laboratory, Hitachi, Ltd.
Kokubunji, Tokyo 185, Japan

Abstract

An SOI CMOSFET with a variable threshold-voltage (V_{th}) is proposed for fabricating power-managed low-power and high-speed sub-1-V ULSIs. An experimental SOI CMOS ring-oscillator with 0.7-μm-long gates and a variable-V_{th} function, fabricated using 0.5-μm processes, showed 46% shorter propagation delay than that for bulk CMOSs and 29% shorter delay than that for conventional SOI CMOSs' under 1-V-operation with almost the same power consumption. These remarkable improvements result from the 0.5-V-lower variable V_{th} and larger drain current of the SOI CMOSFET.

Introduction

Progress in ULSI technologies has led to the introduction of portable information terminals, such as PDAs and PDCs. These portable information terminals require low-power and high-speed ULSIs because of their weak power-source and their need for massive data processing. Several power management schemes have therefore been introduced. We have developed a variable-V_{th} SOI MOSFET using a simple process that fits these scheme. This MOSFET has the largest drain current (I_{ds}) in active mode with the same current-leakage in stand-by mode of all bulk- and SOI-MOSFETs, as shown in Fig. 1.

Fabrication Process Steps

The fabrication process steps are shown in Fig. 2. First, the back gate electrodes are simply formed by P-ion implantation in a p^+ Si substrate (with a concentration of 3×10^{17} cm^{-3}) through a 60-nm-thick Si layer and a 100-nm-thick buried SiO_2 layer. This enables independent substrate biases, i.e., positive biases for nMOSFETs and negative biases for pMOSFETs, to be applied through the back gate electrodes and the p^+ Si substrate. As only adding one mask process and one ion implantation process enables to make the variable V_{th} SOI CMOSFETs, the process is much simpler compared with the previously reported[1]. The LOCOS process is used to achieve isolation, followed by 12-nm-thick gate-SiO_2 formation, comparatively deep non-uniform channel implantations[2], and WSi_2/poly Si dual-gate-electrode formation, i.e., n^+ poly Si for nMOSFETs and p^+ poly Si for pMOSFETs. Finally, W and Al layers are formed for the 1st and 2nd level wirings, respectively.

Experimental results

Figure 3 shows the simulated back-gate-voltage (V_{bg}) dependence on V_{th} of SOI nMOSFETs with SOI thicknesses of 20 to 70 nm. The same channel implantations with a BF_2 dose of 3×10^{12} cm^{-2} were applied to all devices. The simulated results show that a 2-V V_{bg} change results in an approximately 0.35-V V_{th} change for these devices.

The experimental V_{th} values before and after V_{bg} biasing in the fabricated SOI CMOSFETs are shown as a function of effective channel length (L_{eff}) in Fig. 4. The V_{th} values for bulk CMOSFETs are also shown. A V_{bg} of -2 V was chosen for the normal condition in the pMOSFETs because this value corresponds to the normal condition of a pMOSFET in an SOI CMOS inverter with a grounded substrate operating at 2 V. The measured V_{th} shifts of about -/+ 0.5 V for long-channel n- and pMOSFETs after V_{bg} biasing are much larger than previously reported [1] [3] because of our devices' comparatively thicker gate oxide and thinner buried oxide. The values are large enough for power-managed applications.

The drain current in the V_{bg}-biased SOI MOSFETs showed 30% (n-ch) and 24% (p-ch) more current than those in unbiased (0 V for n-ch and -2 V for p-ch) SOI devices, as shown in Fig. 5.

A photograph of a 51-stage unloaded CMOS ring-oscillator (R/OSC) with fabricated back-gate electrodes is shown in Fig. 6. The propagation delay (t_{pd}) of the R/OSCs with 0.5-μm-long and 0.7-μm-long gates is shown in Fig. 7 as a function of the power supply voltage (V_{cc}). The t_{pd} decreased after biasing the back gates. The difference in t_{pd} between biased (high-speed mode) and unbiased (low-power mode) R/OSCs with 0.5-μm-long gates at V_{cc} = 1 V was about 20 ps/gate (18% t_{pd} in low-power mode), while that at V_{cc} = 2 V was only 6 ps/gate (3% t_{pd} in low-power mode). The smaller the V_{cc}, the larger the t_{pd} decrease. The 0.7-μm-gate R/OSC showed a much better t_{pd}. The t_{pd} difference at V_{cc} = 1 V became 60ps/gate (29% t_{pd} in low-power mode) and that at V_{cc} = 2 V became 17 ps/gate (15% t_{pd} in low-power mode). These improvements result from the smaller V_{th}-lowering characteristics of 0.7-μm nMOSFETs, as shown in Fig. 4.

Discussion

When considering a portable information terminal using power-managed ULSIs, the speed in high-speed mode and the power consumption in low-power mode should be defined as those for the terminal itself. (Here we assume the terminal usually operates in low-power mode.) Figure 8 compares the propagation delay of a bulk CMOS R/OSC with that of a power-managed SOI CMOS R/OSC, which usually operates in low-power mode and operates in high-speed mode only when required. The t_{pd} of the power-managed R/OSC with 0.7-μm gates operating at V_{cc} = 1 V was about 54% that of the bulk R/OSC under almost the same power consumption. Moreover, in the SOI CMOS ring-oscillator, the t_{pd} improvement is better in the lower V_{cc} region.

Table 1 summarizes the t_{pd}s and power consumptions of bulk and SOI CMOS R/OSCs operating under various conditions. The power-managed SOI R/OSC showed superior characteristics both in t_{pd} and power consumption.

Conclusion

We have proposed a variable-V_{th} SOI-CMOSFET with simple implanted back-gate electrodes and have fabricated one using 0.5-μm processes. These CMOSFETs showed 0.5-V lower V_{th} and 30% (n-ch) and 24% (p-ch) more current in high-speed mode, i.e., when the back gates are biased, compared with those in a low-power (standard) mode. The propagation delay of a power-managed SOI CMOS ring-oscillator with 0.7-μm-long gates operating at V_{cc} = 1 V was about 46% smaller than that of a bulk R/OSC under almost the same power consumption. In the SOI CMOS ring-oscillator, the t_{pd} improvement is better in the lower V_{cc} region.

Acknowledgment

We are grateful to the Process Technology Development Division of the Central Research Laboratory, Hitachi Ltd., for device fabrication.

References

[1] I. Y. Yang et al., "Back Gated CMOS on SOIAS for Dynamic Threshold Voltage Control", 1995 IEDM Tech. Dig. p. 877

[2] G. G. Shahidi et al., "A Room Temperature 0.1μm CMOS on SOI", IEEE Trans. on Electron Device, 41, p. 2405 (1994)

[3] Jian Chen, et al., "A High Speed SOI Technology with 12ps/18ps Gate Delay Operating at 5V/1.5V", 1992 IEDM Tech. Dig. p. 35

 0-7803-3342-X/96/$5.00©1996 IEEE

BEST AVAILABLE COPY

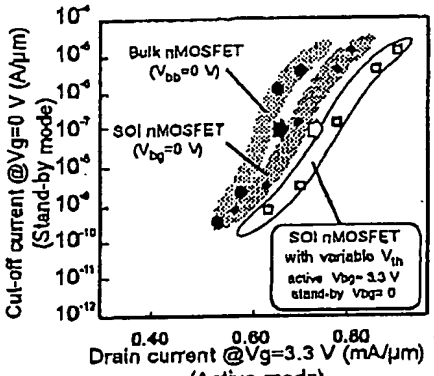

Figure 1 Comparison of performance of variable threshold-voltage SOI MOSFETs and a bulk MOSFET (simulation).

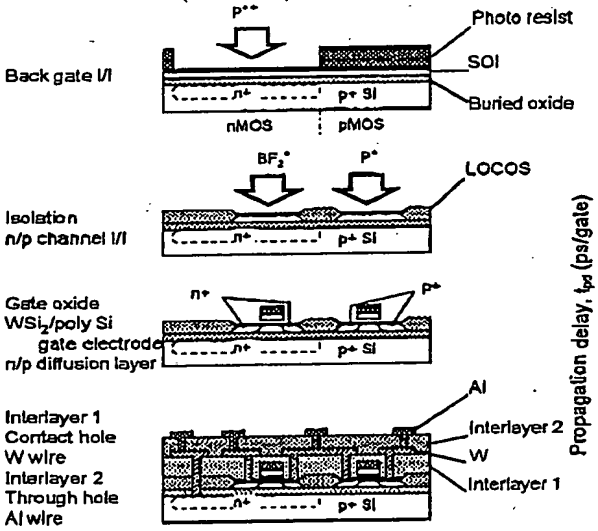

Figure 2 Process flow of variable threshold-voltage SOI CMOSFET.

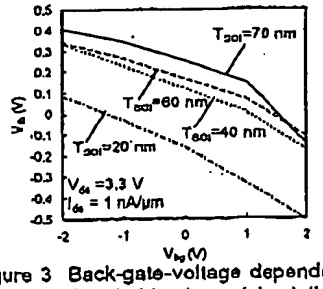

Figure 3 Back-gate-voltage dependence on threshold voltage (simulation).

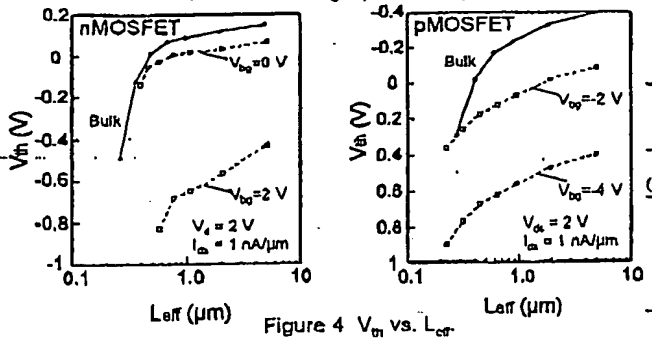

Figure 4 V_{th} vs. L_{eff}.

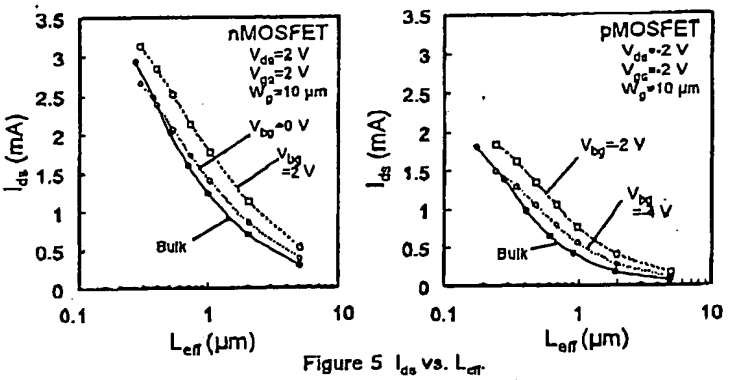

Figure 5 I_{ds} vs. L_{eff}.

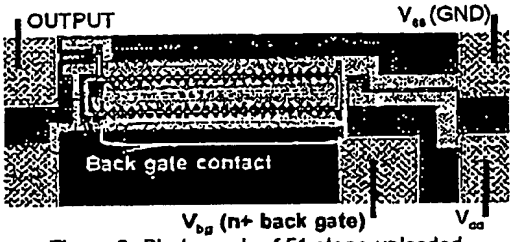

Figure 6 Photograph of 51-stage unloaded CMOS ring oscillator.

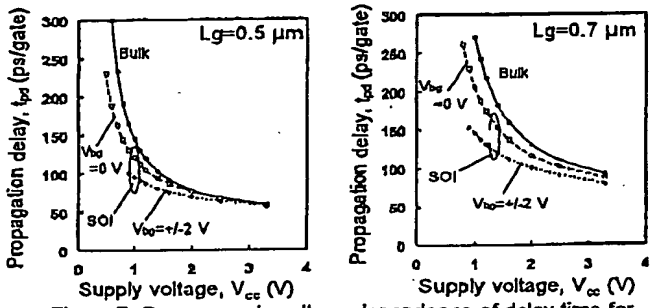

Figure 7 Power-supply-voltage dependence of delay time for one gate.

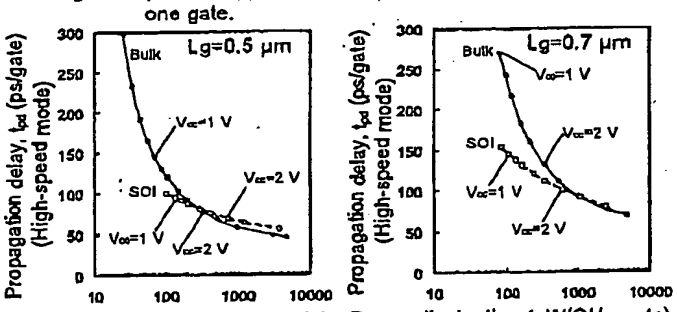

Figure 8 Propagation delay (high-speed mode) vs. power dissipation (low-power mode).

Table 1 Propagation delay and power dissipation.

	V_{cc} = 1 V		V_{cc} = 2 V	
	Delay time ps/gate	Power μW/GHz·gate	Delay time ps/gate	Power μW/GHz·gate
SOI CMOS (power-managed mode)	145	105	100	619
Bulk CMOS	271	96.3	131	347
SOI CMOS (low-power mode)	205	105	117	619
SOI CMOS (high-speed mode)	145	1020	100	2047

* L_g = 0.7 μm

BEST AVAILABLE COPY